REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claims 1-11 were presented for consideration in this application. By the foregoing amendment, Applicant has amended Claims 3 and 8. New Claims 12-16 have been added. Claims 1-16 are now pending.

Applicant thanks the Examiner for acknowledgment of applicant's claim for foreign priority based on an application filed in EPO on 8/21/00 and 3/29/01. Certified copies of the EP 00402331.3 and EP 01400818.9 applications were mailed to the USPTO March 11, 2003.

Claim 3 is amended to clarify that it represents an additional step. Claim 8 is amended to correct a minor antecedence error.

Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Lim US Patent No. 6,430,640 or 35 U.S.C. 102(b) as being anticipated by Suzuki et al. (Suzuki) US Patent No. 4,400,771.

Neither Lim nor Suzuki teach or even suggest the novel arbitration method and apparatus claimed in Applicant's base Claims 1, 7 and 8. Applicant agrees that Lim and Suzuki both teach dynamically assigning a first priority value to each processor in a multiprocessor system. (Lim: Col 15, lines 9-29; Suzuki: Col 5, lines 17-20) However, neither reference suggests "providing two priority values along with each access request from each device" as recited in Claim 1 and similarly in base Claim 7 or "arbitration circuitry connected to receive a request signal from each request output along with an **access priority value** from each access priority register and an **address priority value** from each memory management unit" as recited by base Claim 8.

Regarding Claim 1, Lim's teaching at Col 4, line 9-10 merely indicates that "various priorities can be assigned" but has no indication the two priority values are provided by each device on each request. Lim's description at Col 13, lines 1-12 again makes no reference to two priority values from each device being used for arbitration. Lim does teach how to break a tie but this section does not teach providing two priority values along with each request. (Col 15, lines 30-56) Applicant's embodiment also has a tie breaker mechanism described at paragraphs [39]

and [61], for example, but this tie breaker mechanism is not referred to as the "two priority values" as claimed. Similarly, Suzuki's teaching at Col 4, lines 32-35 make no mention of two priority values. Suzuki's only priority value is stored in register 22 (Fig 2) or register 322 (Fig 3) While Suzuki does teach storing two bits for each priority value, this is just a two-bit code and not two priority values. (Col 5, lines 46-50) Claim 1 is therefore allowable over either reference.

Regarding base Claim 7, neither reference suggests "a plurality of devices connected to access the shared resource, wherein each device has a request output and circuitry for providing **two separate variable priority values"** as recited by Claim 7. Lim's teaching at Col 4, line 9-10 merely indicate that "various priorities can be assigned" but has no indication the two priority values are provided by each device on each request. Lim's description at Col 13, lines 1-12 again makes no reference to two priority values from each device being used for arbitration. Similarly, Suzuki's teaching at Col 4, lines 32-35 make no mention of two priority values. Suzuki's only priority value is stored in register 22 (Fig 2) or register 322 (Fig 3). Claim 7 is therefore allowable over either reference.

Regarding base Claim 8, neither reference suggests "a plurality of memory management units ... has an output for an **address space priority value** contained in each page entry; and arbitration circuitry connected to receive a request signal from each request output along with an **access priority value** from each access priority register and an **address space priority value** from each memory management unit, wherein the arbitration circuitry is operable to schedule access to the shared resource according to the access priority value and the address space priority value." Neither reference has any suggestion of such a memory management unit as explained at paragraph [62] and elsewhere in Applicant's specification. Lim discusses allowing a transfer of a block of data before relinquishing access" but this has nothing to do with a priority value. (Col 2, lines 34-46) Suzuki teaches how to "decode an address assigned to the register circuit 57" but this is no more than accessing a memory mapped register, as is commonly known. (Col 5, lines 38-42) Claim 8 is therefore allowable over either reference.

Dependent Claims 2-6 and 9-11 depend directly or ultimately on an allowable base Claims 1 or 8 and are therefore allowable for this reason and by virtue of their further distinctive recitations.

Regarding Claim 3, neither reference has any suggestion of "providing an address space priority value with each request" as recited in Claim 3 and explained at paragraph [62] and elsewhere in Applicant's specification. Lim discusses allowing a transfer of a "block of data before relinquishing access" but this has nothing to do with a priority value. (Col 2, lines 34-46) Suzuki teaches how to "decode an address assigned to the register circuit 57" but this is no more than accessing a memory mapped register, as is commonly known. (Col 5, lines 38-42)

Regarding Claim 4, neither reference suggests assigning and storing address space priority values in entries of a memory management unit, as discussed above.

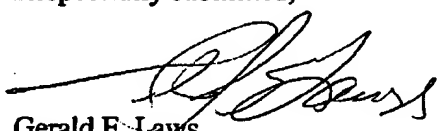
Regarding Claim 5, since neither references suggests providing two priority values from each device, then neither reference can suggest "selecting a higher priority value from each of the two priority values from each device" as recited in Claim 5.

New method Claims 12-16 have been added to more fully protect Applicant's contribution to the art. These Claims depend directly or ultimately on allowable base Claim 1 and are therefore also allowable for this reason and by virtue of their further distinctive recitations regarding establishing a software priority state and access priority value as described in paragraphs [34] to [61] in the specification, for example.

Applicant believes this application and the claims herein to be in a condition for allowance and respectfully requests that the Examiner allow this application to pass to the issue branch.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,



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